PR6244E

Green-power Current Mode PWM Power Switch

GENERAL DESCRIPTION

PR6244E is a current Mode power switch, exhibit extra low standby power consumption (<75mW).

PWM switching frenquency at normal operation is internally fixed. At no load or light load condition, It operates in hiccup mode to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

PR6244E offers power on soft start control and rich protection coverage with auto-recovery features including VDD under voltage lockout (UVLO), VDD over voltage protection (OVP), Cycle-by-Cycle current limiting (OCP), over load protection (OLP), over temperature protection (OTP).

Excellent EMI performance is achieved with PR6244E proprietary frequency hiccup technique. The frequency at below 22KHZ is minimized to avoid audible noise during operation.

PR6244E is offered in DIP-8L package.

FEATURES

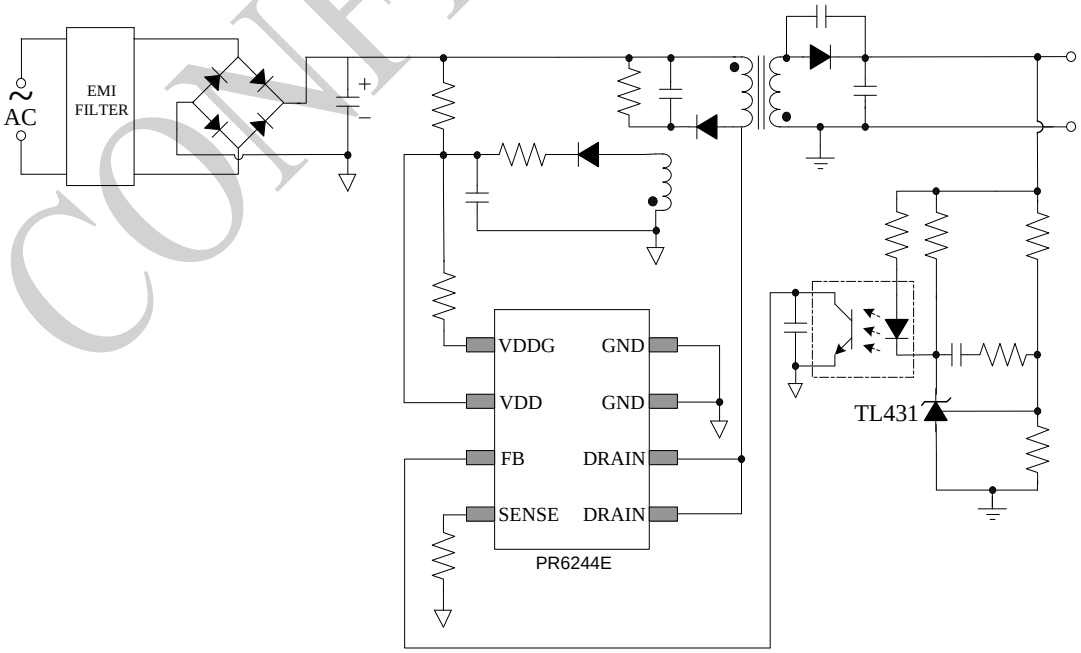
- Extra Low Standby (<75mW)
- Power on Soft Startup
- Frequency spreading to Minimize EMI
- Audible Noise Free Operation
- Fixed 50KHz Switching Frequency
- Comprehensive Protection
  - VDD Under Voltage Lockout with Hysteresis (UVLO)
  - Cycle-by-cycle Over Current Protection (OCP)
  - Overload Protection (OLP) with Auto-recovery
  - Over Temperature Protection (OTP)
  - VDD Over Voltage Protection (OVP)

APPLICATIONS

Offline AC/DC Flyback Converter For

- AC/DC Adapter
- PDA Power Supplies
- Digital Cameras and Camcorder Adapter
- VCR, SVR, STB, DVD&DVCD Player SMPS
- Set-Top Box Power
- Auxiliary Power Supply for PC and Server
- Open-frame SMPS

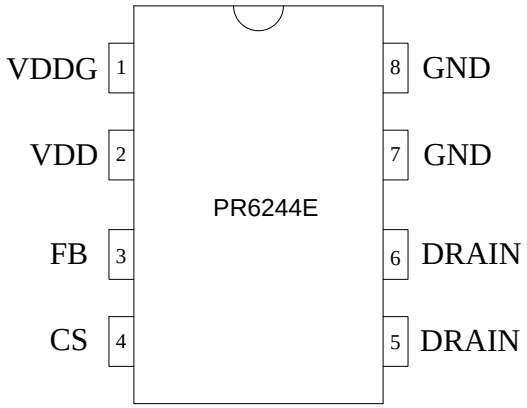
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The PR6244E is offered in DIP-8L package, shown as below.



Parameter	Value
Drain Voltage (off state)	-0.3 to BVdss
VDD DC Supply Voltage	-0.3 to 30V
VDDG DC Supply Voltage	-0.3 to 30V
VDD Zener Clamp Voltage[Note]	VDD_Clamp+0.1V
VDD DC Clamp Current	10 mA
FB Input Voltage	-0.3 to 7V
CS Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T_J	-40 to 150 ℃
Min/Max Storage Temperature T_{stg}	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

Note: VDD_Clamp has a nominal value of 26.5V.

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended period may affect device's reliability.

Package Dissipation Rating

Package	Rja(℃/W)
DIP-8L	65

Absolute Maximum Ratings

ERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	VDDG	P	Internal Gate Driver Power Supply
2	VDD	P	IC DC power supply Input
3	FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at Pin 4.
4	CS	I	Current sense input
5/6	GND	P	Ground
7/8	DRAIN	O	HV MOSFET Drain Pin. The Drain pin is connected to the primary lead of the transformer.

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min/Max	Unit
VDD	VDD Supply Voltage	10.5 to 23.5	V
T_A	Operating Ambient Temperature	-20 to 85	℃

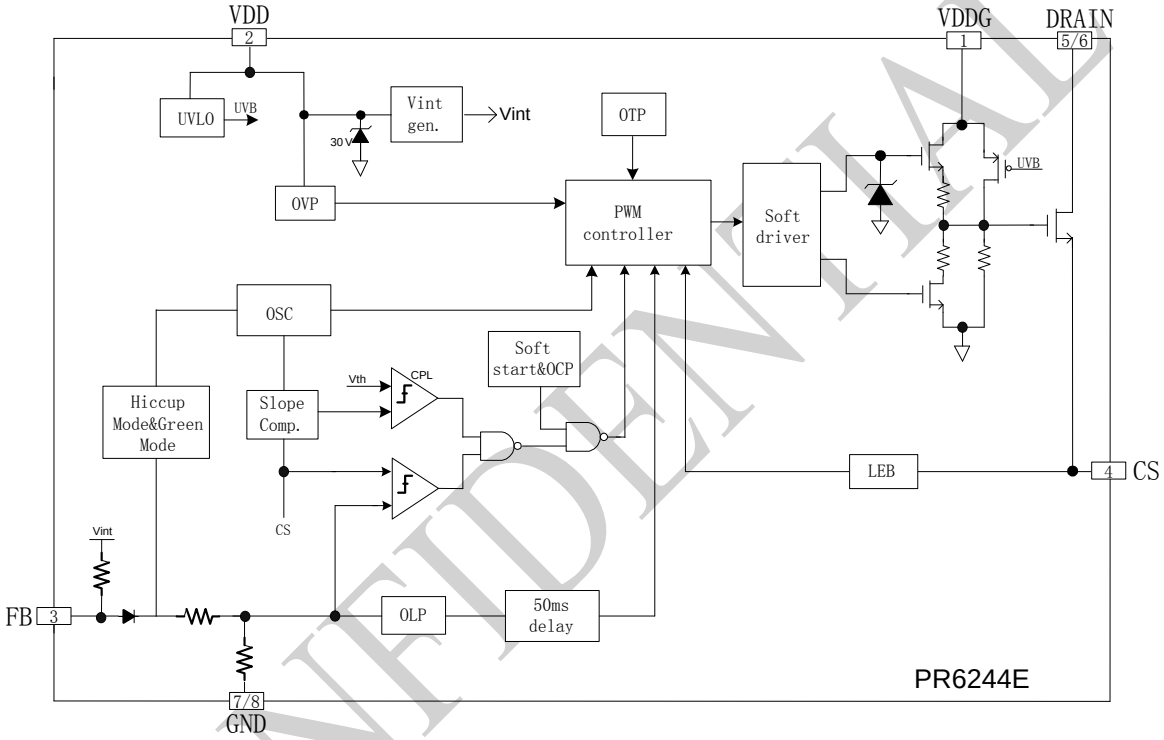
Output Power Table

	Package	230VAC ±15%	85-265VAC
		Open Frame[1]	Open Frame[1]
PR6244E	DIP-8L	15W	12W

Notes:

1. Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sink, at 50℃ ambient.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

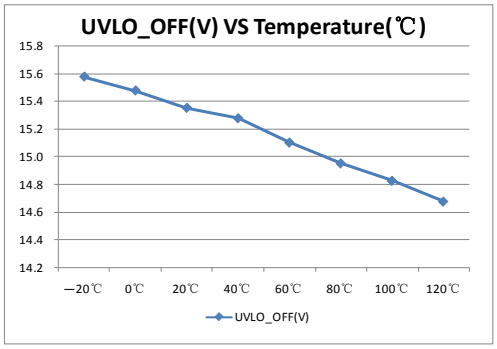
(TA = 25 ℃,VDD=16V, unless otherwise noted)

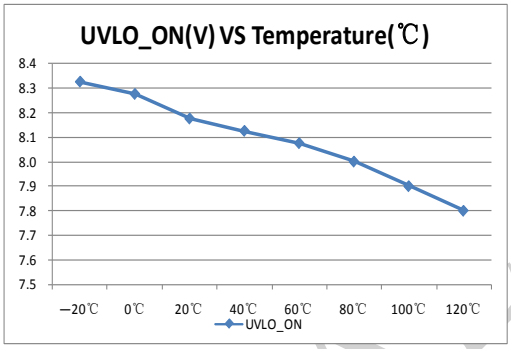
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD)						
Ist	VDD Start up Current	VDD=UVLO_OFF-1 V, measure leakage current into VDD		0.5	1	μA
I_VDD_Operation	Operation Current	V_{FB}=3V		1.35	1.40	mA
	Hiccup Mode Current	VDD=16V, V_{FB}=1V		420	450	μA
UVLO(ON)	VDD Under Voltage Lockout Enter		7.2	8.2	9.2	V
UVLO(OFF)	VDD Under Voltage Lockout Exit (Recovery)		14.3	15.3	16.3	V
VDD_Clamp		I_{VDD}=10mA		32.0		V
OVP_ON	Over voltage protection voltage	FB=3V Ramp up VDD until gate clock is off	28.1	29.1	30.1	V
Feedback Input Section(FB Pin)						
VFB_Open	VFB Open Loop Voltage			4.5		V
Avcs	PWM input gain ΔVFB/ ΔVCS			1.71		V/V
Maximum duty cycle	Max duty cycle		75	80	85	%
Vref_green	The threshold enter green mode			1.7		V
Vref_HH	The threshold exit hiccup mode			1.23		V
Vref_HL	The threshold enter hiccup mode			1.20		V
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND and measure current		300		μA
VTH_PL	Power Limiting FB Threshold Voltage			3.5		V
TD_PL	Power limiting Debounce Time		50	60	70	mSec
Z_{FB}_IN	Input Impedance			16		Kohm
Current Sense Input(CS Pin)						
SST	Soft start time			5		ms
T_blanking	Leading edge blanking time			300		ns
Z_{SENSE}_IN	Input Impedance			40		Kohm
T_D_OC	Over Current Detection and Control Delay	From Over Current Occurs till the gate driver output starts to turn off		120		nSec
V_{TH}_OC	Current Limiting Threshold Voltage with zero duty cycle			0.76		V
Vocp_clamping	Current limiting threshlod at			0.90		V

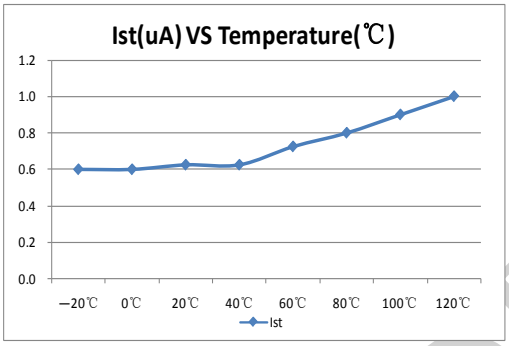
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	maximum Duty					
Oscillator						
F_{OSC}	Normal Oscillation Frequency @ FB=3V		45	50	55	KHz
△f_OSC	Frequency jittering			+/-4		%
F_shuffling	Shuffling frequency			25		Hz
△f_Temp	Frequency Temperature stability			2		%
△f_VDD	Frequency Voltage Stability			1		%
F_Hiccup	Hiccup Mode Switch Frequency			22		KHz
MOSFET Section						
BVdss	MOSFET Drain-Source Breakdown voltage		600			V
Rdson	Static, Id=1.0A				4.4	Ω
On Chip OTP						
OTP	Over temperature protection trip point with Recommended PCB layout.			145		℃

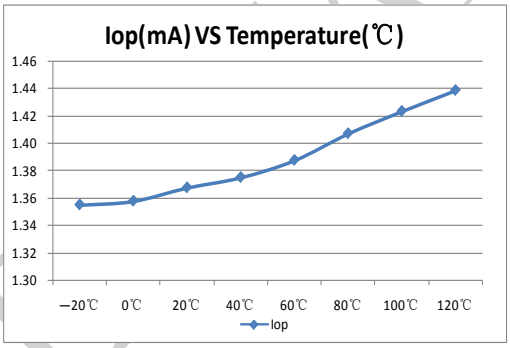
CHARACTERIZATION PLOTS

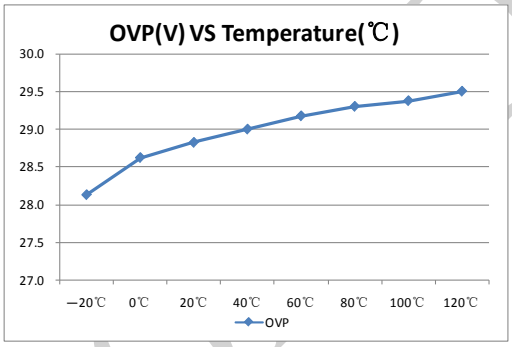
VDD = 16V, TA = 25 ℃ condition applies if not otherwise noted.

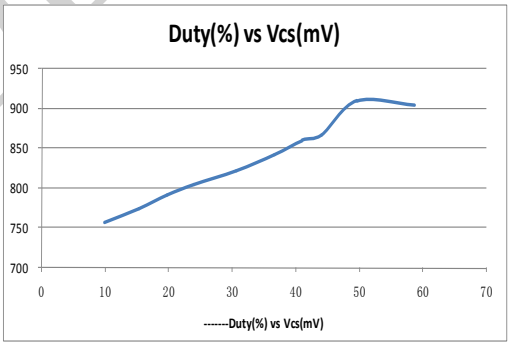


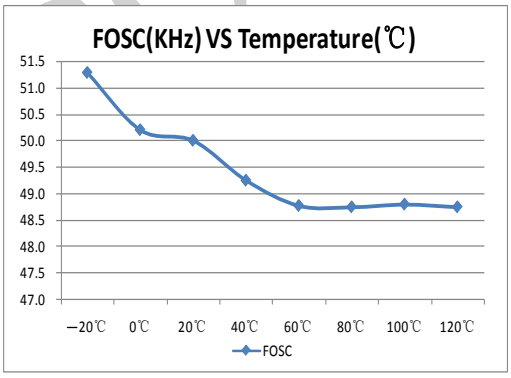












OPERATION DESCRIPTION

PR6244E is a highly integrated current mode PWM Power Switch optimized for high performance, extra low standby power consumption and cost effective offline flyback converter applications. The 'hiccup mode' control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

Startup Current and Start up Control
Startup current of PR6244E is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application. For AC/DC adaptor with universal input range design, a 4 MΩ, 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and yet low power dissipation design solution.

Operating Current
The Operating current of PR6244E is 1.35mA. Good efficiency is achieved with this low operating current together with the 'hiccup mode' control features. The operation current is greatly reduced at no/light conditions such that extra low standby can be achieved.

Soft Start
PR6244E features an internal typical 5ms soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO (OFF), the primary winding current is controlled to be gradually increased to the maximum level. Every restart up is followed by a soft start.

Frequency spreading for EMI improvement
The frequency spreading (switching frequency modulation) is implemented in PR6244E. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Green Mode Operation
PR6244E provides green-mode control to reduce the switching frequency in light-load and no-load conditions. $V_{FB,}$ which is derived from the voltage feedback loop, is taken as the reference. Once V_{FB} is lower than the threshold voltage (Vref_green), switching frequency is continuously decreased to the minimum green-mode frequency of around 22 KHz.

Extended Hiccup Mode Operation
At light load or zero load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy.

The switching frequency is internally adjusted at no load or light load condition. The switching frequency is reduced at light/no load condition to improve the conversion efficiency. At light load or no load condition, the FB input drops below hiccup mode threshold voltage (Vref_H_L) and device enters Hiccup Mode control. The gate driver output switches only when FB voltage is higher than the threshold voltage (Vref_H_H) to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

The switching frequency control also eliminates the audible noise at any loading conditions.

Oscillator Operation
The switching frequency is internally fixed at 50KHz. No external frequency setting components are needed for PCB design simplification.

Current Sensing and Leading Edge Blanking
Cycle-by-Cycle current limiting is offered in PR6244E current mode PWM control. The switching current is detected by a sense resistor connected to the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spikes due to snubber diode reverse recovery and surge gate current of power MOSFET at initial internal power MOSFET on state. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking

period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation
Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and eliminates the subharmonic oscillation and thus reduces the output ripple voltage.

Driver
The internal power MOSFET in PR6244E is driven by a dedicated gate driver for power switching control. Too weak the gate driver results in higher conduction and switch loss of power MOSFET while too strong gate driver results in the compromise of EMI.

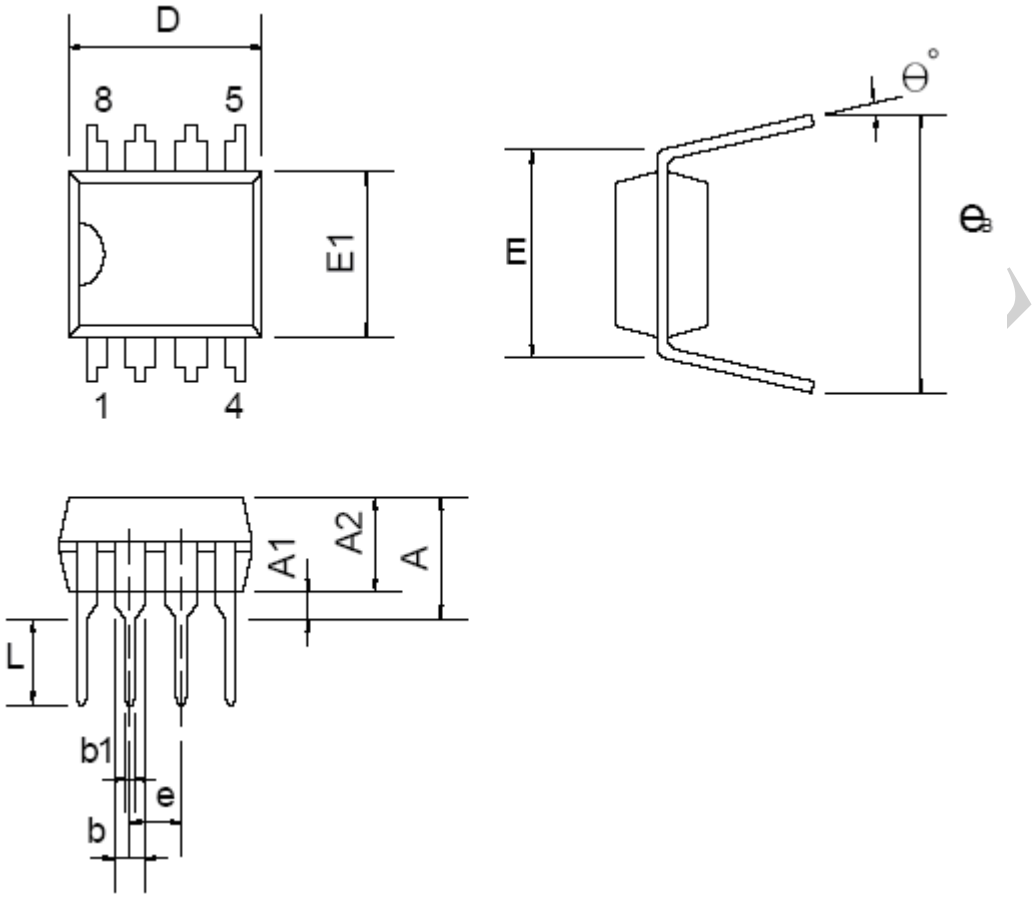
A good tradeoff is achieved through the built-in totem pole gate design with well controlled output strength and dead time control. The low idle loss and good EMI system design is achieved with this dedicated control scheme.

Protection Controls
Good power supply system reliability is achieved with auto-recovery protection features including VDD under voltage lockout (UVLO), VDD over voltage protection (OVP), Cycle-by-Cycle current limiting (OCP), over load protection (OLP), over temperature protection (OTP). The OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range.

At overload condition, when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit shuts down the converter. It restarts when VDD voltage drops below Vth_recovery.

Package Dimensions

DIP-8L



Dimensions

Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.334			0.210
A1	0.381			0.015		
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524			0.060	
b1		0.457			0.018	
D	9.017	9.271	10.160	0.355	0.365	0.400
E		7.620			0.300	
E1	6.223	6.350	6.477	0.245	0.250	0.255
e		2.540			0.100	
L	2.921	3.302	3.810	0.115	0.130	0.150
eB	8.509	9.017	9.525	0.335	0.355	0.375
θ°	0°	7°	15°	0°	7°	15°